

Fig. 1A PRIOR ART

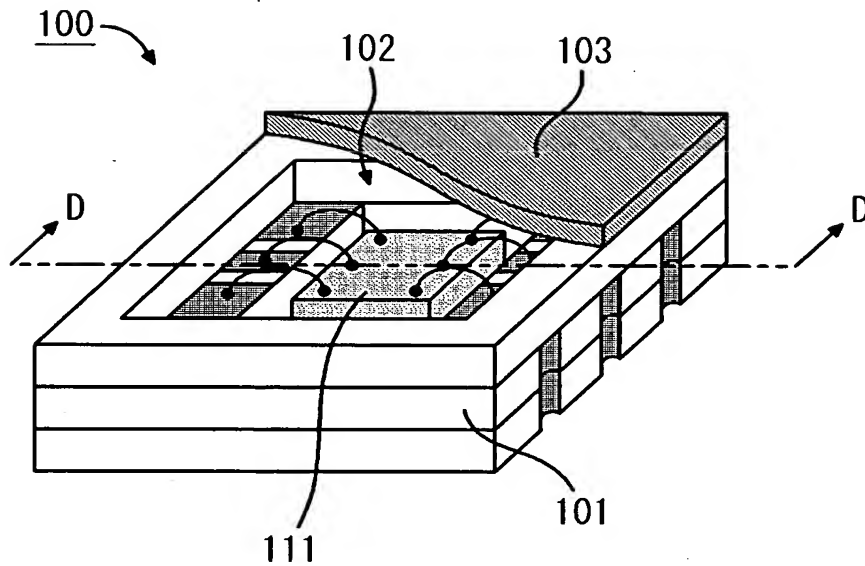


Fig. 1B PRIOR ART

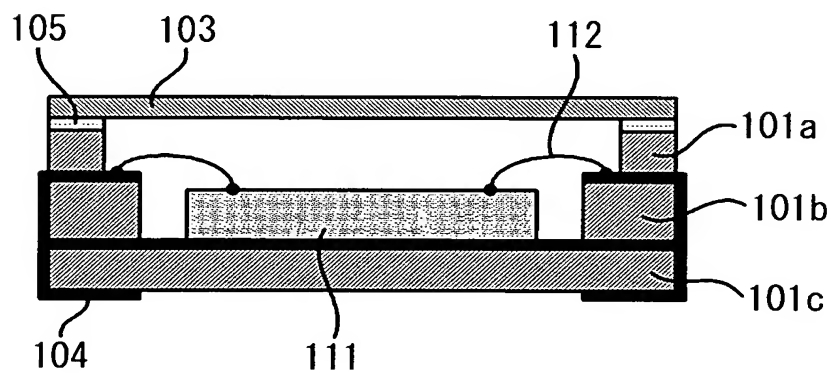


Fig. 2A PRIOR ART

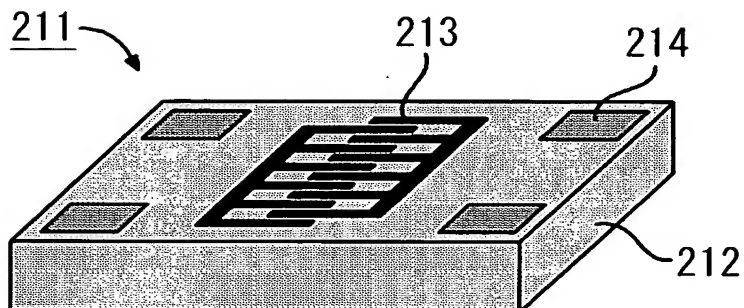


Fig. 2B PRIOR ART

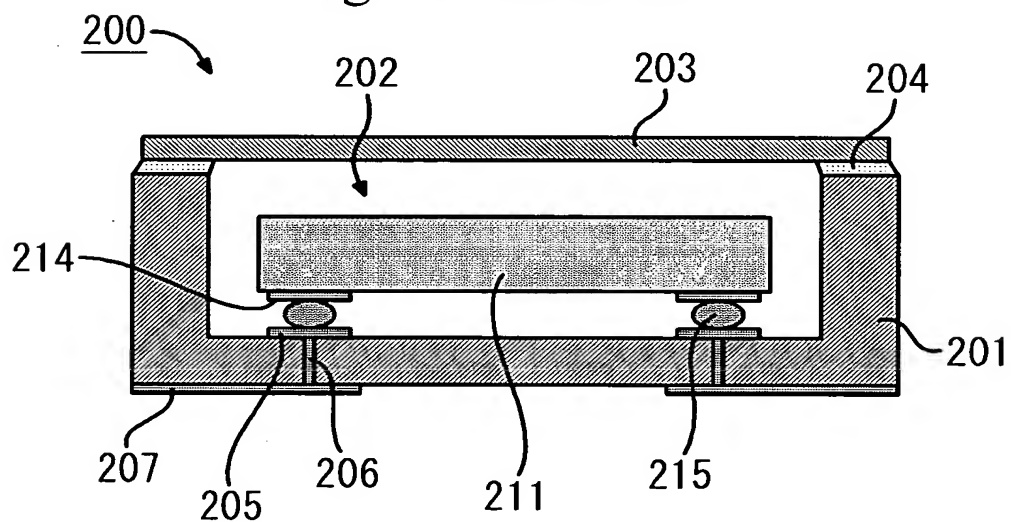


Fig. 3A PRIOR ART

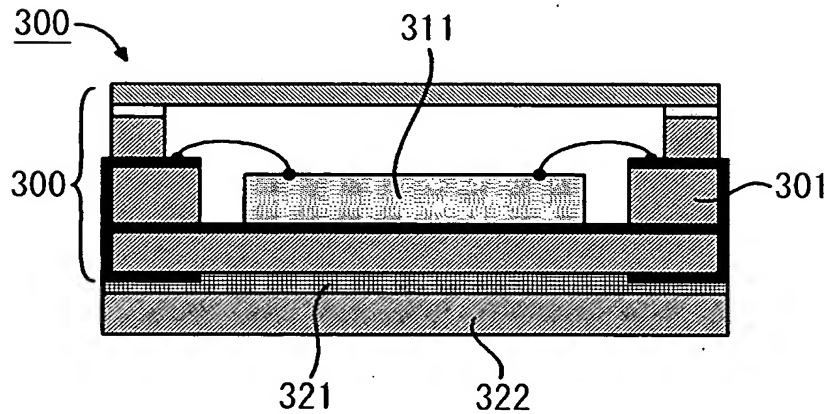


Fig. 3B PRIOR ART

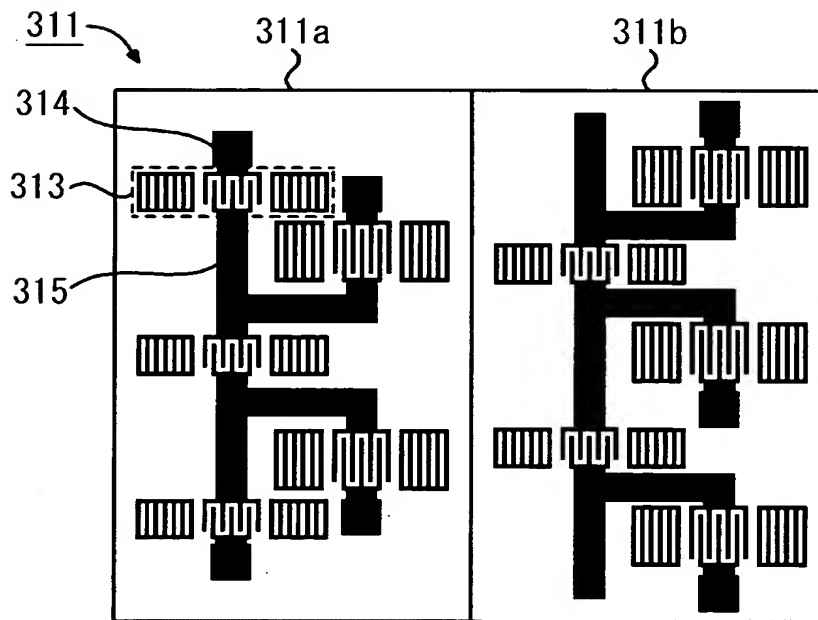


Fig. 4A

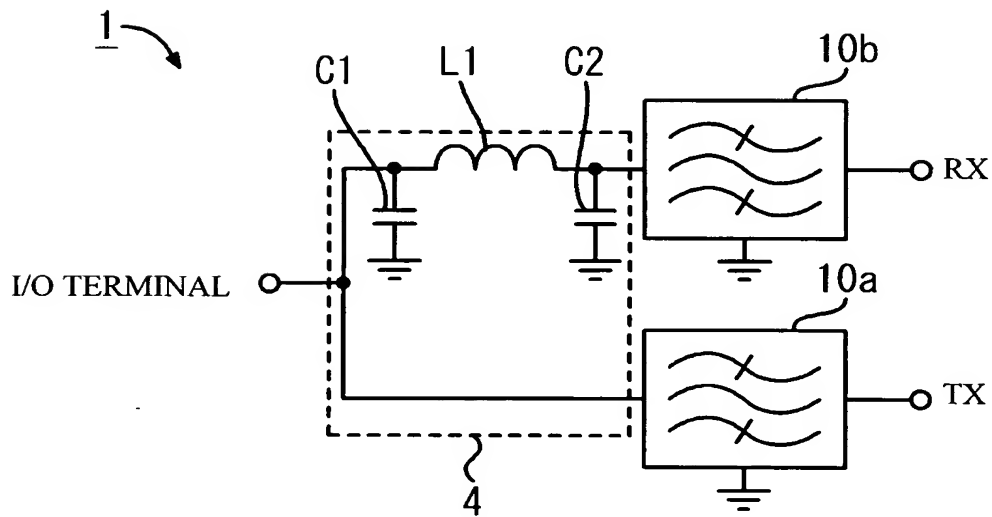


Fig. 4B

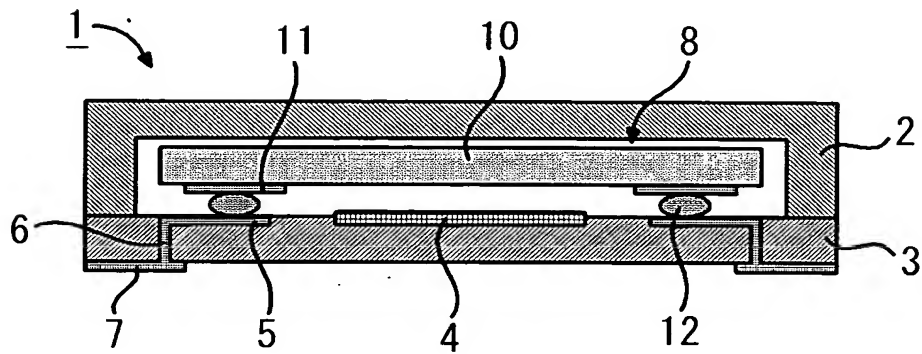


Fig. 5A

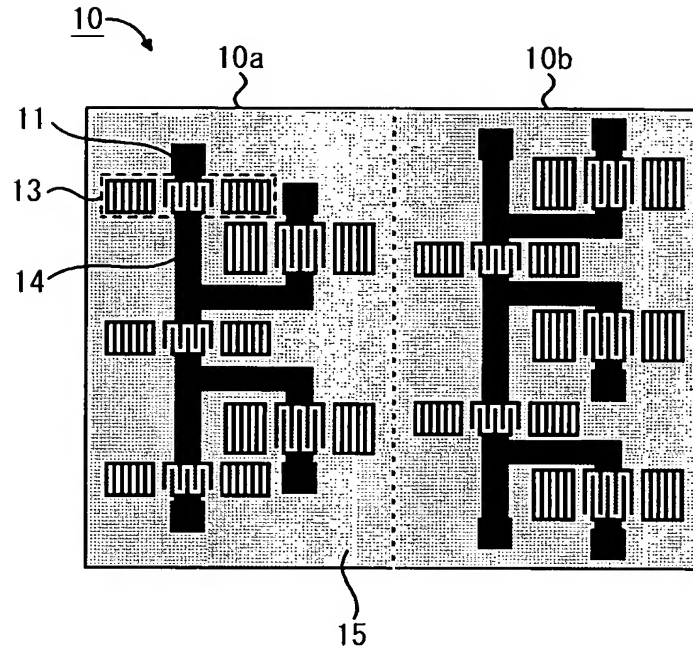


Fig. 5B

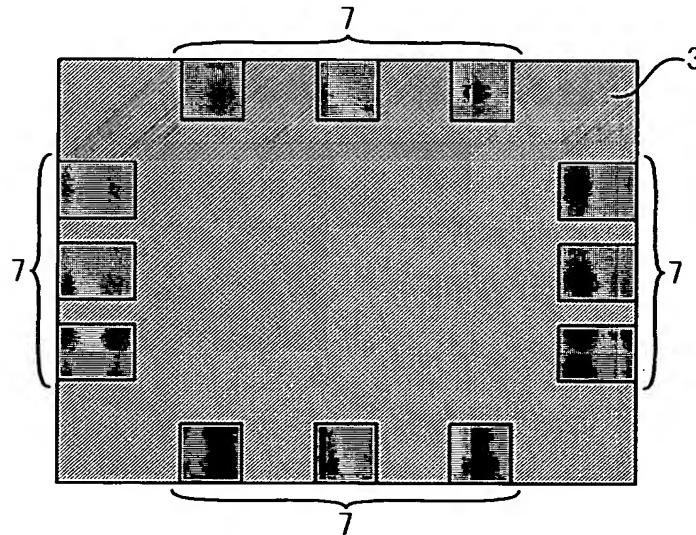


Fig. 6A

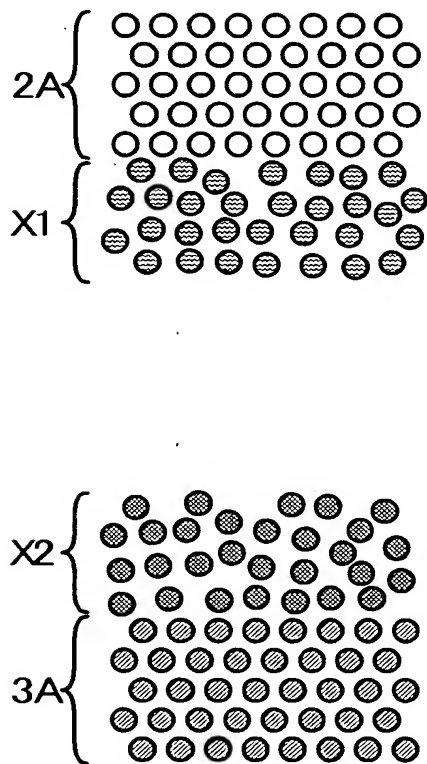


Fig. 6B

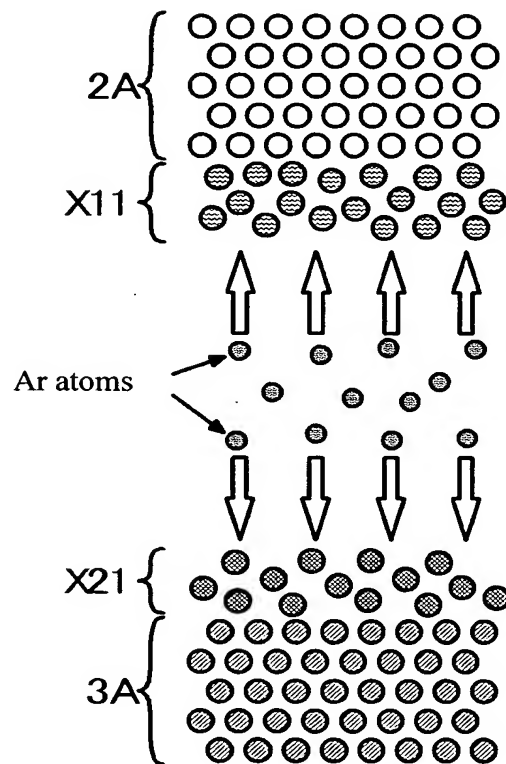


Fig. 7A

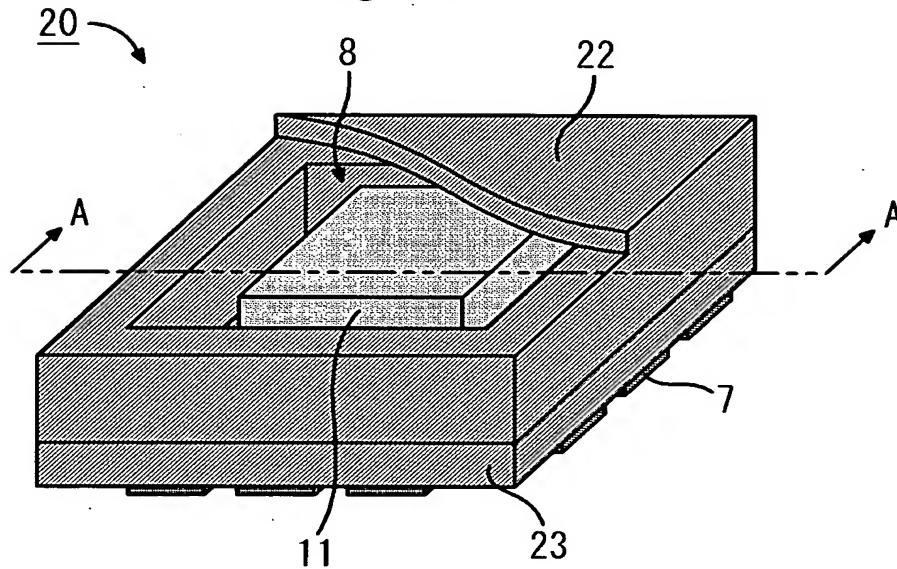


Fig. 7B

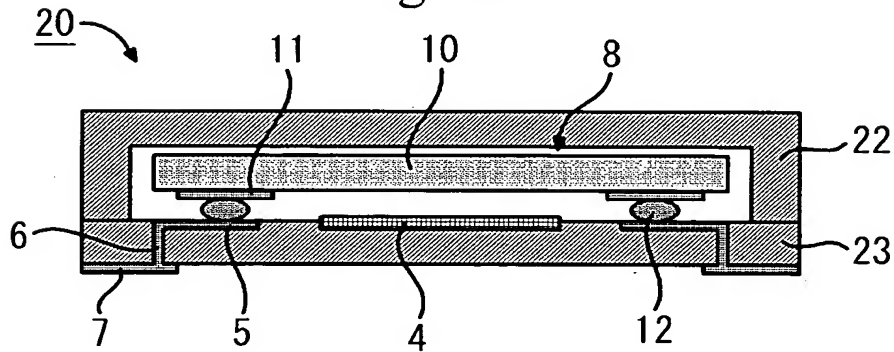


Fig. 8A

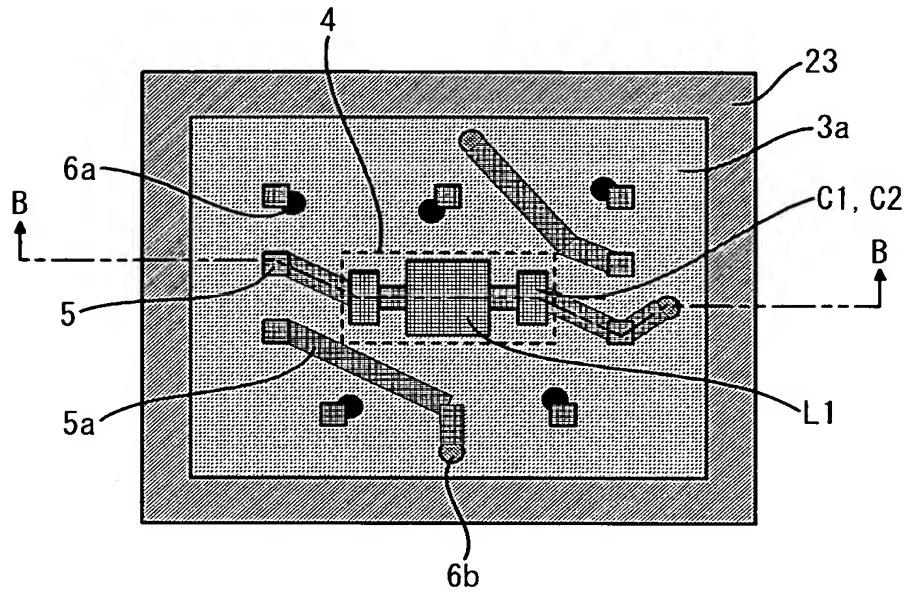


Fig. 8B

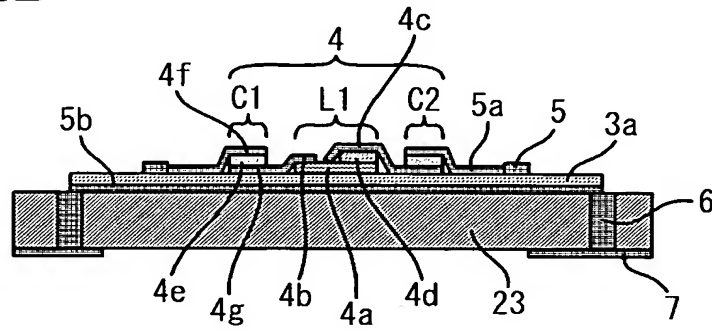


Fig. 8C

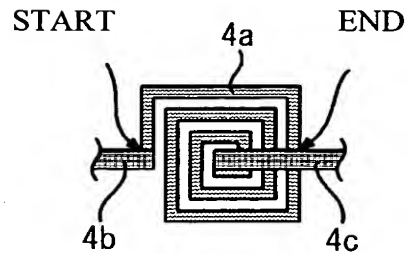


Fig. 8D

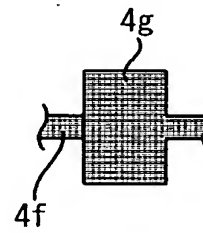


Fig. 9A

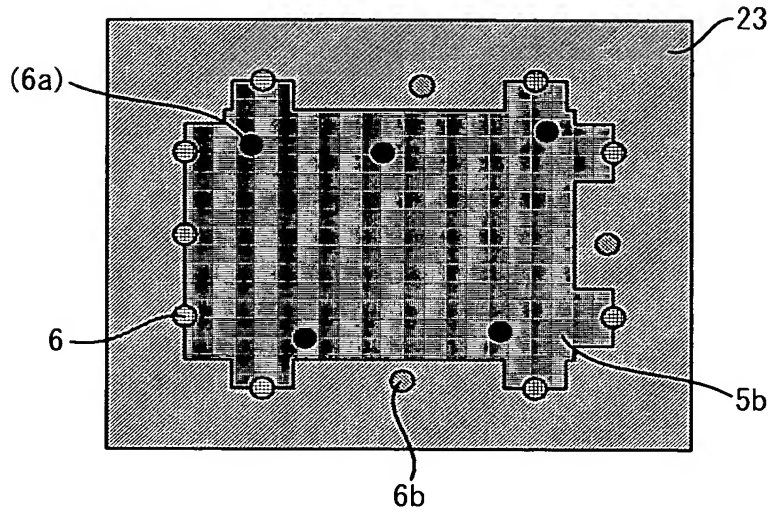
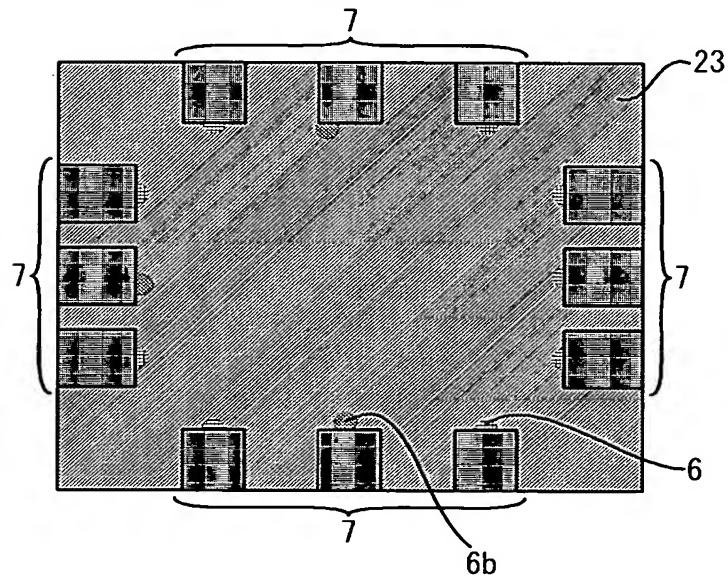


Fig. 9B



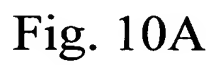
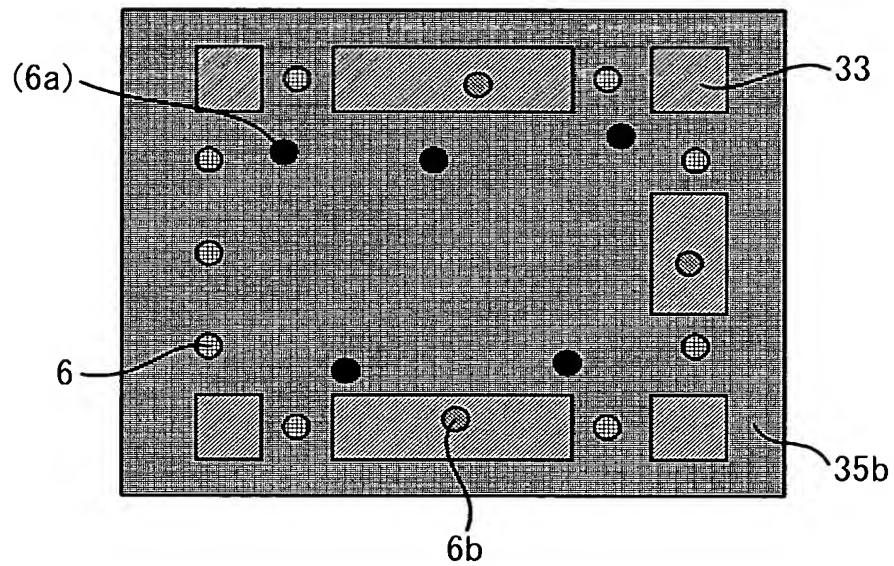


Fig. 11



Inventor's Name: UEDA et al
Application No.: New Application
Docket No.: 025720-00030

A cross-sectional view of a semiconductor device 40. The device features a substrate 7 with a base layer 6. A central layer 4 is flanked by side regions 5 and 12. A top layer 10 is positioned above the central region, with a patterned layer 11 on top of it. The entire structure is enclosed by a top layer 42 and side walls 43. A layer 48 is located between the central layer 4 and the top layer 10. The side walls 43 are labeled 43a at the top and 43b at the bottom. The top layer 42 is labeled 42a at the top and 42b at the bottom.

Fig. 13

